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Sir:

Transmitted herewith for filing under 37 CFR 1.53(b) is the

- ☒ patent application of
☐ continuation patent application of
☐ divisional patent application of
☐ continuation-in-part patent application of

Inventor(s)/Applicant Identifier: **Kouichi Takahashi, Kenichi Kasai, Takahiro Daikoku, Takayuki Uda, Toshitada Netsu, Takeshi Yamaguchi, Takahiko Matsushita, and Osamu Maruyama**

For: Sealing Structure for Multi-chip Module

- ☒ This application claims priority from each of the following Application Nos./filing dates:
Japanese Patent Application No. 11-162046, filed June 9, 1999
the disclosure(s) of which is (are) incorporated by reference.
- ☐ Please amend this application by adding the following before the first sentence: "This application is a ☐ continuation ☐ continuation-in-part of and claims the benefit of U.S. Application No. 60/_____, filed _____, the disclosure of which is incorporated by reference."

Enclosed are:

- ☒ 6 page(s) of specification
☒ 3 page(s) of claims
☒ 1 page of Abstract
☒ 3 sheet(s) of ☒ formal ☐ informal drawing(s).
- ☐ An assignment of the invention to _____
- ☒ A ☐ signed ☒ unsigned Declaration & Power of Attorney
- ☐ A ☐ signed ☐ unsigned Declaration.
- ☐ A Power of Attorney by Assignee with Certificate Under 37 CFR Section 3.73(b).
- ☐ A verified statement to establish small entity status under 37 CFR 1.9 and 37 CFR 1.27 ☐ is enclosed ☐ was filed in the prior application and small entity status is still proper and desired.
- ☐ A certified copy of a _____ application.
- ☐ Information Disclosure Statement under 37 CFR 1.97.
- ☐ A petition to extend time to respond in the parent application.
- ☐ Notification of change of ☐ power of attorney ☐ correspondence address filed in prior application.

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TOTAL	

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x \$78.00 =	\$
+ \$260.00 =	
TOTAL	\$690.00

Respectfully submitted,
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PATENT APPLICATION

Sealing Structure for Multi-chip Module

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Sealing Structure for Multi-chip Module

BACKGROUND OF THE INVENTION

This invention relates to a sealing and cooling mechanism for multi-chip modules, and more particularly to a sealing structure for multi-chip modules formed by hermetically sealing high-performance semiconductor devices over a substrate for use in computers and the like.

Along with the continuing increase in the processing speed and storage capacity of computers, semiconductor devices are increasingly faster and more densely integrated. At the same time, however, the increase in heat emitted by semiconductor devices resulting from their growing power consumption is posing a problem, together with the problem of reliability of stable operation of semiconductor devices. Especially in multi-chip modules wherein a large number of semiconductor devices are mounted over a substrate wired in high density, this increased heating poses a major challenge to configure a satisfactory cooling structure.

On the other hand, to maintain the environmental stability of semiconductor devices and their cooling performance as modules for long periods, how to configure a sealing structure which can hermetically enclose semiconductor devices and He gas for enhancing the efficiency of thermal conduction within multi-chip modules is a major technical problem. One known sealing structure for multi-chip modules is disclosed in, for instance, "MCM-D/C Application for High Performance Module," *Proceedings of 1996 International Conference on Multi-chip Modules*, pp. 69-74.

This sealing structure is described below with reference to Fig. 5. In Fig. 5, a large number of semiconductor devices 12 are mounted over a wiring board 11 consisting of alumina ceramic. On the bottom side of the wiring board 11 are provided input/output pins 13. A cap board 16 consisting of a highly thermally conductive materials, covering the wiring board 11, is fixed to the circumference of the wiring board 13 with solder 18 to hermetically seal the module. Between the semiconductor devices 12 and the cap board 16 is provided a thermally conductive means, known as thermally

conductive compounds 14, each matching one or another of the semiconductor devices 12, to transmit the heat emitted by the semiconductor devices 12 to the cap board. Over the top surface of the cap board 16 is fitted an air-cooled heat sink 17 to radiate heat from the semiconductor devices 12 transmitted via the cap board 16.

5 The above-described sealing structure for multi-chip modules involves several problems of reliability of the sealing connection and cooling performance. In the above-cited structure described in "MCM-D/C Application for High Performance Module," *Proceedings of 1996 International Conference on Multi-chip Modules*, pp. 69-74, highly thermally conductive metals, such as aluminum and copper, are used for the
10 cap and the heat sink to secure satisfactory cooling performance.

On the other hand, a ceramic material, such as alumina ceramic, is used for the wiring board to facilitate fine multi-layered wiring. Because aluminum and copper constitute the cap board or heat sink, and have higher rates of thermal expansion than ceramics, the disparity in thermal expansion between the cap board and heat sink on the
15 one hand and the wiring board on the other hand, widens with an increase in the overall heat emission of the modules and/or in the wiring board size. Because the cap board and the wiring board are fixed with solder in the described structure, deformation in the horizontal direction is constrained with the solder-fixed part as the constraining point as the difference in thermal expansion between the cap board and the wiring board increases.

20 The quantity of thermal deformation with respect to a module of 150 mm square in size, using aluminum ($24 \times 10^{-6}/^{\circ}\text{C}$ in thermal expansion coefficient) for the cap and alumina ceramic ($7 \times 10^{-8}/^{\circ}\text{C}$ in thermal expansion coefficient) for the wiring board is calculated below. Whereas semiconductor devices are usually cooled to keep their temperature at or below 80°C , the temperature of the wiring board then is about 80°C ,
25 and that of the cap, around 60°C , though it may vary with the cooling method. Therefore, the relative quantity of thermal deformation against a temperature change from the normal level from the center to a corner of the module can be calculated by the following equation (1):

$$\Delta L = LX (\alpha_1 \cdot \Delta T_1 - \alpha_2 \cdot \Delta T_2) \quad (1)$$

30 ΔL : Relative quantity of thermal deformation

L: Length of member (= $150/\sqrt{2}$)

α_1 : Linear expansion coefficient of wiring board (= $7 \times 10^{-6}/^{\circ}\text{C}$)

ΔT_1 : Temperature change of wiring board (= $80 - 20 = 60^{\circ}\text{C}$)

α_2 : Linear expansion coefficient of cap ($= 24 \times 10^{-6}/^{\circ}\text{C}$)

ΔT_2 : Temperature change of cap ($= 60 - 20 = 40^{\circ}\text{C}$)

The relative quantity of thermal deformation predicted by using Equation (1) is $57 \mu\text{m}$. If this relative quantity in the horizontal direction is constrained, the module will be bent in the vertical direction by a bimetal effect, resulting in an expanding gap between the cap and the wiring board. Thus, the gap in the thermally conductive compound part applied between the cap and the semiconductor devices will increase, deteriorating the cooling performance, making it more difficult to maintain at a satisfactory level. Moreover, as this thermal deformation gives rise to a large stress in the solder-fixed portion as well, the ceramic and/or the solder part may be destroyed, reducing reliability as well.

SUMMARY OF THE INVENTION

The present invention improves the above-noted problematic aspects of the prior art and provides a sealing structure for multi-chip modules, which enhances reliability while providing superior cooling performance. In one embodiment, a structure is provided in which materials subject to significant elastic deformation, such as rubber and plastics, intervene in fastening parts between members differing in thermal expansion. The deformation of these elastic materials absorbs the relative thermal deformation between the members along with variations in temperature. In another embodiment a structure is provided in which smoothly sliding materials, such as plastics, intervene in the fastening part between members differing in thermal expansion and the sliding of these materials absorbs the relative thermal deformation between the members with variations in temperature.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1. illustrates a cross section of a sealing and cooling mechanism for multi-chip modules in a first preferred embodiment;

Fig. 2 illustrates a cross section of a sealing and cooling mechanism for multi-chip modules in a second preferred embodiment;

Fig. 3 illustrates a cross section of a sealing and cooling mechanism for multi-chip modules in a third preferred embodiment;

Fig. 4 illustrates a cross section of a sealing and cooling mechanism for multi-chip modules in a fourth preferred embodiment; and

Fig. 5 illustrates a cross section of a sealing and cooling mechanism for multi-chip modules according to the prior art.

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DESCRIPTION OF THE SPECIFIC EMBODIMENTS

Fig. 1 is a cross section of a sealing structure for multi-chip modules, illustrating the configuration of a first preferred embodiment of the invention. In the structure of Fig. 1, a large number of semiconductor devices 2 are mounted over a wiring board 1 consisting of a ceramic material. The wiring board 1 consists of a material which is compatible with the semiconductor devices 2 in thermal expansion rate. On the bottom side of the wiring board 1 are provided input/output pins 3.

The under face of a frame 5, consisting of a ferronickel alloy which is compatible with the wiring board 3 in thermal expansion rate, is mutually engaged by a solder bond 8 with the face of the wiring board 1 over which the semiconductor devices 2 are mounted.

The upper part of the frame 5 extends outside the wiring board 1, and the upper face of the frame 5 constitutes a flange face in which an O- ring groove is cut. The upper and lower faces of the circumference of an air-cooled heat sink 7, consisting of aluminum, copper or the like, a material incompatible with the frame 5 in thermal expansion rate, constitute flange faces, and a highly elastic rubber O-ring 15 is placed between the under flange face and the upper O-ring-grooved face of the frame 5.

Hermetic sealing is achieved by placing a plastic member 6 excelling in relative sliding ease over the upper face of the circumference of the air-cooled heat sink 7 to restrain the upper face of the plastic member 6 at the inside middle stage of an upper frame 10 and fastening together the lower part of the upper frame 10 and the frame 5 with bolts 9 to squeeze the rubber O-ring 15.

A gap allowing for the precision of assembly and the difference in thermal expansion is provided between the side face of the inside middle stage of the upper frame 10 and that of the circumference of the air-cooled heat sink 7, and a fine gap is provided between the upper face of the frame 5 and the under face of the circumference of the air-cooled heat sink 7 to avoid their contact while maintaining the hermetic sealing provided by the rubber O-ring 15. Thus deformation of the module in its vertical direction is

restrained by preventing the air-cooled heat sink 7 from constraining relative thermal deformation in the horizontal direction of the upper frame 10, frame 5 and wiring board 1.

Between the air-cooled heat sink 7 and the semiconductor devices 2 are provided thermally conductive compounds 4, each matching one or another of the semiconductor devices 2. By restraining the deformation of the modules in the vertical direction, the spacing of the thermally conductive compounds 4 is kept constant to secure a high level of cooling performance. Further, the stress occurring in the solder bond 8 engaging the frame 5 and the wiring board 1 with each other is reduced, and a high level of connection reliability of the sealing part is thereby secured.

Fig. 2 is a cross section of a sealing structure for multi-chip modules, illustrating the configuration of a second preferred embodiment of the invention. This second embodiment is the same as the first embodiment except that another rubber O-ring 15 is provided over the circumference of the air-cooled heat sink 7 and an O-ring groove is cut into the inside middle stage of the upper frame 10. In other words, the second rubber O-ring 15 is used in place of the plastic member 6 in Fig. 1.

Fig. 3 is a cross section of a sealing structure for multi-chip modules, pertaining to a third preferred embodiment of the invention. In this third embodiment, an O-ring groove is provided in each of the middle stage of the frame 5 and the under face of the upper frame 10, and fastening is accomplished on the circumference of the air-cooled heat sink 7 with bolts 9 via rubber O-rings 15. Further, between the side face of the middle stage of the frame 5 and that of the periphery of the air-cooled heat sink 7, the positioning of the air-cooled heat sink 7 in the horizontal direction is set via a rubber member 19, which is elastic enough to absorb the difference in thermal expansion between the frame 5 and the heat sink 7. This embodiment is the same as the first embodiment, except in these respects.

Fig. 4 is a cross section of a sealing structure for multi-chip modules, pertaining to a fourth preferred embodiment of the invention. In this fourth embodiment, a highly hermetic and elastic packing 20 is used in place of the rubber O-rings 15 and rubber member 19 in the third embodiment, and the frame is clear of the O-ring groove. In other respects, this embodiment is the same as the third embodiment.

The present invention makes it possible to realize a sealing structure for multi-chip modules which can achieve a high packaging density for semiconductor devices emitting high temperature heat and high reliability for sealing connection.

[illegible]

What is claimed is:

- 1 1. A sealing structure for multi-chip modules, comprising:
2 a wiring board having one face mounted with a plurality of semiconductor
3 devices and another face having connecting pins arranged thereover;
4 a frame having a thermal expansion rate compatible with that of the wiring
5 board, provided on the circumference of that face of the wiring board mounted with the
6 semiconductor devices;
7 a cap covering the plurality of semiconductor devices, the cap having a
8 thermal expansion rate different from that of the frame;
9 a heat conducting material provided between the plurality of
10 semiconductor devices and the cap for transmitting heat generated by the plurality of
11 semiconductor devices to the cap;
12 an attachment for fixing the frame and the wiring board to each other; and
13 an intervening member disposed between the frame and the cap for joining
14 the frame and the cap to each other.
- 1 2. A sealing structure for multi-chip modules as in claim 1 wherein
2 the intervening member comprises an elastic substance.
- 1 3. A sealing structure for multi-chip modules as in claim 2 wherein
2 the intervening member comprises an O-ring.
- 1 4. A sealing structure for multi-chip modules as in claim 2 wherein
2 the intervening member comprises packing.
- 1 5. A sealing structure for multi-chip modules as in claim 1 wherein
2 the intervening member comprises a sliding member.
- 1 6. A sealing structure for multi-chip modules as in claim 5 wherein
2 the sliding member comprises plastic material.
- 1 7. A sealing structure for multi-chip modules as in claim 1 wherein
2 the cap comprises an air-cooled heat sink.

1 8. A sealing structure for multi-chip modules as in claim 1 wherein
2 the wiring board comprises a ceramic material, the cap comprises at least one of
3 aluminum and copper, and the frame comprises a ferronickel alloy.

1 9. A sealing structure for multi-chip modules comprising:
2 a wiring board having one face mounted with a plurality of semiconductor
3 devices and another face having connecting pins arranged thereover;
4 a first frame having a thermal expansion coefficient compatible with that
5 of the wiring board, the first frame provided on a periphery of the face of the wiring board
6 mounted with the semiconductor devices;
7 a second frame disposed over the first frame;
8 a cap having a circumference and having a thermal expansion coefficient
9 different from that of the first and second frames and covering the plurality of
10 semiconductor devices;
11 a heat conducting material disposed between the cap and the plurality of
12 semiconductor devices for transmitting heat from the semiconductor devices to the cap;
13 an attachment to fix the first frame and the wiring board to each other; and
14 a fastener for fastening the first and second frames and the cap together via
15 an intervening member.

1 10. A sealing structure for multi-chip modules as in claim 9 wherein
2 O-ring grooves are provided in one face of the first frame and one face of the second
3 frame, and the cap is fastened between the first frame and the second frame using at least
4 one O-ring.

1 11. A sealing structure for multi-chip modules as in claim 10 wherein
2 an elastic member is provided between a side face of the cap and a face of the first frame.

1 12. A sealing structure for multi-chip modules as in claim 9 wherein
2 elastic packing is provided between the first frame and the second frame so as to cover
3 the circumference of the cap.

1 13. A method of sealing multi-chip modules which modules include a
2 wiring board over which a plurality of semiconductor devices are mounted, a frame

3 provided on a periphery of the wiring board, and a cap having a periphery which cap
4 covers the plurality of semiconductor devices, comprising:
5 attaching a lower face of the frame to a face of the wiring board over
6 which the semiconductor devices are mounted;
7 placing an O ring between an upper face of the frame and a lower face of
8 the periphery of the cap;
9 placing a plastic member to make possible relative sliding between the
10 upper face of the frame and a lower face of a second frame provided above the first
11 frame;
12 restraining the upper face of the plastic member with the lower face of the
13 second frame; and
14 fastening the first frame and the second frame together.

1 14. A method as in claim 13 wherein a gap is further provided between
2 the side face of the circumference of the cap and that of the inside middle stage of the
3 second frame.

1 15. A method as in claim 13 wherein the first frame and the second
2 frame are mechanically connected together.

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Sealing Structure for Multi-chip Module

ABSTRACT OF THE DISCLOSURE

A sealing structure for multi-chip modules stable in cooling performance and excelling in sealing reliability is to be provided. The under face of a frame 5 compatible with a wiring board 1 in thermal expansion rate is fixed with solder 8 to the face of the wiring board 1 for mounting semiconductor devices 2; a rubber O-ring 15 is placed between the upper face of the frame 5 and the under face of the circumference of an air-cooled: heat sink 7; the plastic member 6 making possible relative sliding is placed between the upper face of the circumference of the heat sink 7 and the upper frame 10; the upper face of a plastic member 6 is restrained with the inside middle stage of an upper frame 10; and the lower part of the upper frame 10 and the frame 5 are fastened together with bolts 9.

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FIG.1

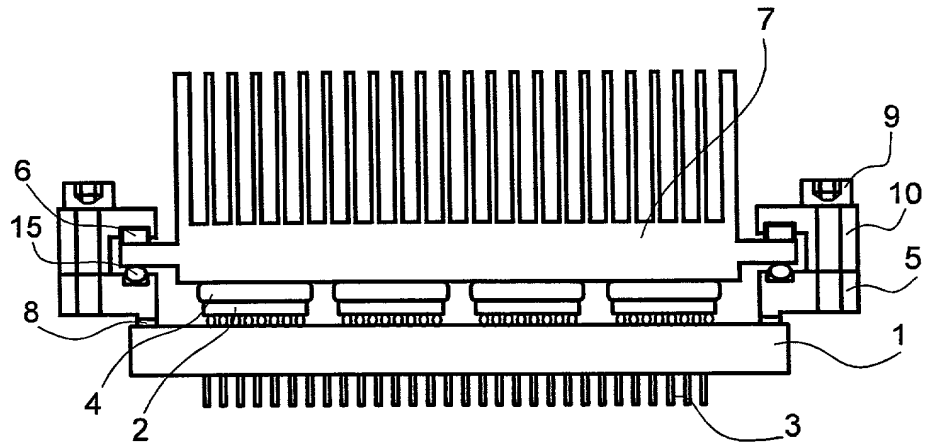


FIG.2

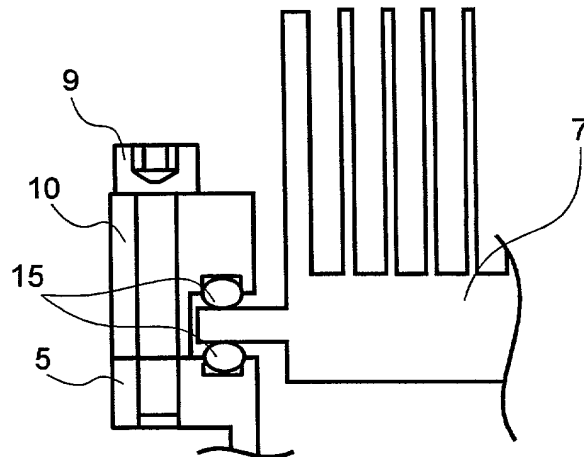


FIG.3

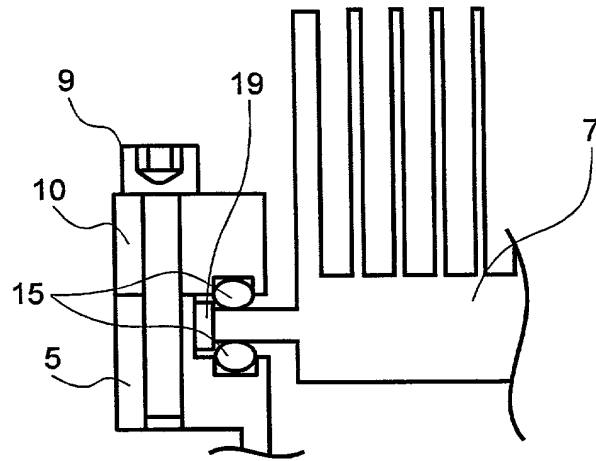


FIG.4

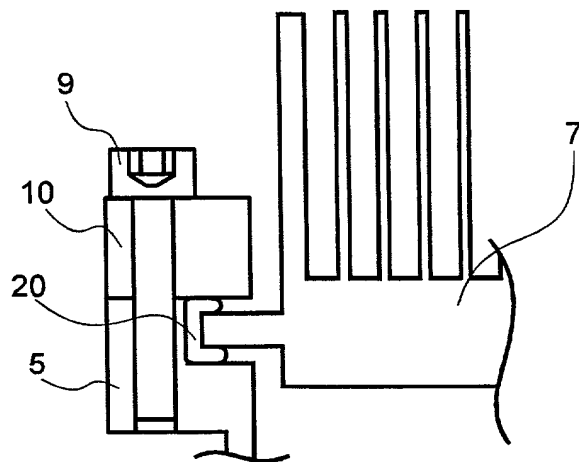
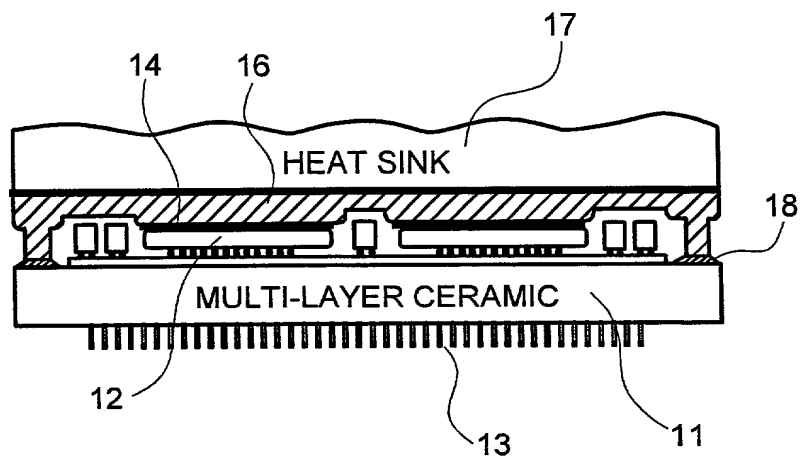


FIG.5



DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I declare that:

My residence, post office address and citizenship are as stated below next to my name; I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: **"Sealing Structure for Multi-chip Module,"** the specification of which was filed on June 9, 2000, as Application No. _____.

I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, Section 1.56. I claim foreign priority benefits under Title 35, United States Code, Section 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)

Country	Application No.	Date of Filing	Priority Claimed Under 35 USC 119
Japan	11-162046	June 9, 1999	Yes

I hereby claim the benefit under Title 35, United States Code § 119(e) of any United States provisional application(s) listed below:

Application No.	Filing Date

I claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, Section 1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

Application No.	Date of Filing	Status

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith.

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I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

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